In the Claims:

Please amend the claims as follows:

Kindly add Claims 2-12.

1. (Currently Amended) A delay lock loop for an FPGA architecture comprising:

a reference delay line having ~~an~~ first input and an output, said first input programmably coupled to a reference clock and selectably coupled through an inverter programmably disposed in series with said reference delay line;

a feedback delay line having an input and an output; said input programmably coupled to a feedback clock and selectably coupled through an inverter programmably disposed in series with said feedback delay line;

~~a divide-by-two circuit having an input and an output, said input coupled to said output of said reference delay line;~~

a phase detector having first input, a second input, and a plurality of outputs, said first input programmably coupled to said output of said ~~divide-by-two circuit~~reference delay line, and said second input coupled to said output of said feedback delay line, wherein said reference delay line and said feedback delay line are selectably coupled to said phase detector through a plurality of divide-by-two circuits;

a control logic circuit having a plurality of inputs and a plurality of outputs, at least one of said plurality of inputs programmably coupled to at least one of said plurality of outputs of said phase detector;

a programmable delay line having a reference clock input, a plurality of data inputs, and an output, said reference clock input coupled to said reference clock, said plurality of data inputs programmably coupled to said plurality of outputs of said control logic circuit to receive data to program a delay in said programmable delay line ~~in the operation of the DLL~~;

a clock doubler having an input and an output, said input programmably coupled to said output of said programmable delay line; and

a clock tree having an input and an output, said input programmably coupled to said output of said clock doubler, and said output forming ~~the~~said feedback clock programmably coupled to said input of said feedback delay line and a clock input of a flip-flop.

2. (New) The delay lock loop as in claim 1, wherein said programmable delay line further comprises:

a secondary delay line having a first input programmably coupled to said reference clock and a second input programmably coupled to said control logic circuit wherein said secondary delay line has a delay period controlled by a plurality of data bits received from said control logic circuit;

a primary delay line having a first input programmably coupled to said an output of said secondary delay line and a second input programmably coupled to said control logic circuit wherein said primary delay line has a delay period controlled by a plurality of data bits received from said control logic circuit; and

a pulse shaper having an input programmably coupled to an output of said primary delay line.

3. (New) The delay lock loop as in claim 1, wherein said reference clock is an external clock.

4. (New) The delay lock loop as in claim 1, wherein said reference clock is an internal clock.

5. (New) The delay lock loop as in claim 2, wherein said secondary delay line is implemented using a delay quanta.

6. (New) The delay lock loop as in claim 2, wherein said primary delay line is implemented using a delay quanta.

7. (New) A method for providing a delay lock loop in an integrated circuit comprising:

providing a reference delay line having a first input and an output, said first input programmably coupled to a reference clock and selectably coupled through an inverter programmably disposed in series with said reference delay line;

providing a feedback delay line having an input and an output; said input programmably coupled to a feedback clock and selectably coupled through an inverter programmably disposed in series with said feedback delay line;

providing a phase detector having first input, a second input, and a plurality of outputs, said first input programmably coupled to said output of said reference delay line, and said second input coupled to said output of said feedback delay line, wherein said reference delay line and said feedback delay line are selectably coupled to said phase detector through a plurality of divide-by-two circuits;

providing a control logic circuit having a plurality of inputs and a plurality of outputs, at least one of said plurality of inputs programmably coupled to at least one of said plurality of outputs of said phase detector;

providing a programmable delay line having a reference clock input, a plurality of data inputs, and an output, said reference clock input coupled to said reference clock, said plurality of data inputs programmably coupled to said plurality of

outputs of said control logic circuit to receive data to program a delay in said programmable delay line;

providing a clock doubler having an input and an output, said input programmably coupled to said output of said programmable delay line; and

providing a clock tree having an input and an output, said input programmably coupled to said output of said clock doubler, and said output forming said feedback clock coupled to said input of said feedback delay line.

8. (New) The method of claim 7, wherein providing a programmable delay line further comprises:

providing a secondary delay line having a first input programmably coupled to said reference clock and a second input programmably coupled to said control logic circuit wherein said secondary delay line has a delay period controlled by a plurality of data bits received from said control logic circuit;

providing a primary delay line having a first input programmably coupled to said an output of said secondary delay line and a second input programmably coupled to said control logic circuit wherein said primary delay line has a delay period controlled by a plurality of data bits received from said control logic circuit; and

providing a pulse shaper having an input programmably coupled to an output of said primary delay line.

9. (New) The method claim 7, wherein said reference clock is an external clock.

10. (New) The method of claim 7, wherein said reference clock is an internal clock.

11. (New) The method of claim 8, wherein said secondary delay line is implemented using a delay quanta.

12. (New) The method of claim 8, wherein said primary delay line is implemented using a delay quanta.